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WHAT IS CLAIMED IS:

1. An apparatus including an interface circuit, the apparatus comprising:

a first device including,

a first receive data terminal,

a first transmit data terminal,

a first power supply terminal configured to convey a first power supply voltage, and

a second power supply terminal configured to convey a second power supply voltage;

a second device including,

a third power supply terminal configured to bear a third power supply voltage different from the first power supply voltage,

a fourth power supply terminal configured to bear a fourth power supply voltage different from the second power supply voltage,

a second receive data terminal configured to convey a received data signal, and

a second transmit data terminal configured to convey a default voltage while the second receive data terminal receives a data signal, the second device interpreting the received data signal traversing a receiver threshold value as a first logic state and interpreting the received data signal not traversing the

receiver threshold value as a second logic state opposite the first logic state, the first power supply voltage traversing the receiver threshold value;

a switch including a first node, a second node, and a control node, the first node in electrical communication with the first transmit data terminal, the second transmit data terminal, and the second receive data terminal, and the second node in electrical communication with the first power supply terminal, and the control node in electrical communication with the first receive data terminal,

wherein the switch is configured to a first state to convey the first power supply voltage to the second receive data terminal, and

wherein the switch is configured to a second state to convey the default voltage signal from the second transmit data terminal to the second receive data terminal, and to convey a voltage signal from the second transmit data terminal to the first receive data terminal.

2. The interface circuit according to claim 1 wherein:

the switch comprises a PMOS transistor;

the first node comprises a drain of the PMOS transistor;

the second node comprises a source of the PMOS transistor; and

the control node comprises a gate of the PMOS transistor.

3. The interface circuit according to claim 1 wherein:

the switch comprises a PNP bipolar transistor;

the first node comprises an emitter of the PNP bipolar transistor;

the second node comprises a collector of the PNP bipolar transistor; and

the control node comprises a base of the PNP bipolar transistor.

4. The interface circuit according to claim 3 wherein:

the second device is an RS232 device having a receiver threshold value of approximately +3V, a low first logic state, a default voltage of -12V, a third power supply terminal configured to bear a third power supply voltage of approximately +12V, and a fourth power supply terminal configured to bear a fourth power supply voltage of approximately -12V.

5. The interface circuit according to claim 4 wherein:

the first device is a TTL microcontroller having a first power supply terminal configured to bear a first power supply voltage of approximately +5V and a second power supply terminal configured to bear a second power supply voltage of approximately ground.

6. The interface circuit according to claim 5 wherein the TTL microcontroller includes a pin addressable eight-bit parallel port and a software program instructing the microcontroller to synchronize and conduct serial-to-parallel conversion

of signals communicated between the RS232 device and the TTL microcontroller.

7. A method of communicating between a first device utilizing a first logic family and a second device utilizing a second logic family different from the first logic family, the method comprising the steps of:

forming an electrical connection between a first node of a switch and a transmit data terminal of the first device;

forming an electrical connection between the first switch node and a transmit data terminal of the second device;

forming an electrical connection between the first switch node and a receive data terminal of the second device;

forming an electrical connection between a second node of the switch and a power supply of the first device;

forming an electrical connection between a control node of the switch and a receive data terminal of the first device;

transmitting a first power supply voltage from the receive data terminal of the first device to the switch control node, such that the switch is placed into a first state and a second power supply voltage is conveyed from the transmit data terminal of the second device to the transmit data terminal of the first device;

transmitting the first power supply voltage from the receive data terminal of the first device to the switch control node, such that the switch is placed

into the first state and a third power supply voltage is conveyed from the transmit data terminal of the second device to the receive data terminal of the second device; and

transmitting a fourth power supply voltage from the receive data pin of the first device to the switch control node, such that the switch is placed into a second state and the first power supply voltage is conveyed from the first device to the receive data pin of the second device, the second device interpreting the received first power supply voltage traversing a receiver threshold value as a first logic state.

8. The method according to claim 7 wherein:

the step of forming an electrical connection between the first switch node and a transmit data pin of the second device comprises forming an electrical connection between the first switch node and a transmit data pin of an RS232 device;

the step of forming an electrical connection between the first switch node and a receive data pin comprises forming an electrical connection between the first switch node and a receive data pin of the RS232 device;

the step of transmitting a first power supply voltage from the receive data pin of the first device to the switch control node causes an RS232 power supply voltage of approximately -12V to be conveyed from the RS232 transmit data pin to the RS232 receive data pin; and

the step of transmitting a fourth power supply voltage from the receive data pin of the first device

to the switch control node causes the first power supply voltage traversing a +3V receiver threshold value to be conveyed to the RS232 receive data pin.

9. The method according to claim 8 wherein:

the step of forming an electrical connection between the first switch node and a transmit data pin of the first device comprises forming an electrical connection between the first switch node and a transmit data pin of a TTL microcontroller;

the step of forming an electrical connection between the second switch node and the power supply comprises forming an electrical connection between the second switch node and a power supply bearing a +5V TTL microcontroller power supply voltage;

the step of forming an electrical connection between the switch control node and a receive data pin of the first device comprises forming an electrical connection between the switch control node and the receive data pin of the TTL microcontroller;

the step of transmitting a first power supply voltage from the receive data pin of the first device to the switch control node comprises transmitting a +5V TTL microcontroller power supply voltage to the switch control node to cause the +5V TTL microcontroller power supply voltage to be conveyed from the RS232 transmit data pin to the receive data pin of the TTL microcontroller; and

the step of transmitting a fourth power supply voltage from the receive data pin of the first device to the switch control node comprises transmitting a 0V TTL microcontroller power supply voltage to the switch control node to cause the +5V TTL

microcontroller power supply voltage traversing the receiver threshold value to be conveyed to the receive data pin of the RS232 device.

10. The method according to claim 7 wherein:

the step of forming an electrical connection between the first switch node and a transmit data pin of the first device comprises forming an electrical connection between a collector of a PNP transistor and the transmit data pin of the first device;

the step of forming an electrical connection between the first switch node and a transmit data pin of the second device comprises forming an electrical connection between the PNP collector and the transmit data pin of the second device;

the step of forming an electrical connection between the first switch node and a receive data pin of the second device comprises forming an electrical connection between the PNP collector and the receive data pin of the second device;

the step of forming an electrical connection between the second switch node and a power supply of the first device comprises forming an electrical connection between an emitter of the PNP transistor and the power supply of the first device; and

the step of forming an electrical connection between a control node of the switch and a receive data pin of the first device comprises forming an electrical connection between a base of the PNP transistor and the receive data pin of the first device.

11. The method according to claim 7 wherein:

the step of forming an electrical connection between the first switch node and a transmit data pin of the first device comprises forming an electrical connection between a drain of a PMOS transistor and the transmit data pin of the first device;

the step of forming an electrical connection between the first switch node and a transmit data pin of the second device comprises forming an electrical connection between the PMOS drain and the transmit data pin of the second device;

the step of forming an electrical connection between the first switch node and a receive data pin of the second device comprises forming an electrical connection between the PMOS drain and the receive data pin of the second device;

the step of forming an electrical connection between the second switch node and a power supply of the first device comprises forming an electrical connection between a source of the PMOS transistor and the power supply of the first device; and

the step of forming an electrical connection between a control node of the switch and a receive data pin of the first device comprises forming an electrical connection between a gate of the PMOS transistor and the receive data pin of the first device.